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# Integrated Circuits Comprising Patterned Functional Liquids

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**Solid-state heterostructures are the cornerstone of modern electronics. To enhance the functionality and performance of integrated circuits, the spectrum of materials used in the heterostructures is being expanded by an increasing number of compounds and elements of the periodic table. While the integration of liquids and solid–liquid interfaces into such systems would allow unique and advanced functional properties and would enable integrated nanoionic circuits, solid-state heterostructures that incorporate liquids have not been considered thus far. Here solid-state heterostructures with integrated liquids are proposed, realized, and characterized, thereby opening a vast, new phase space of materials and interfaces for integrated circuits. Devices containing tens of microscopic capacitors and field-effect transistors are fabricated by using integrated patterned NaCl aqueous solutions. This work paves the way to integrated electronic circuits that include highly integrated liquids, thus yielding a wide array of novel research and application opportunities based on microscopic solid/liquid systems.**

Intriguing phenomena in biology, chemistry, and physics occur when states of matter—solid, liquid, gas, and plasma—are combined. Thus, amazing possibilities would emerge if it were possible to incorporate liquids at microscopic length scales into integrated circuits (for an illustration, see **Figure 1**). Enabling integrated circuitry to include liquids would introduce a new phase of matter to the spectrum of materials currently available for solid-state devices, and thereby qualitatively extend their range of properties and functionalities. Integrated circuits that comprise microscopic liquid volumes will unlock numerous innovative applications of heterostructures in physics, chemistry, and biology.

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**DOI: 10.1002/adma.201802598**

Labs-on-a-chip already combine liquids and solids in microfluidic chips (for an overview, see, e.g., ref. [1]). In labs-on-a-chip, fluids are moved and analyzed, primarily by employing lithographically patterned polymer or silicon structures. Compared to labs-on-a-chip, solid-state heterostructures used in integrated circuits have very different tasks, such as computing, data storage, and control. They therefore draw on different architectures than labs-on-a-chip, are built with different technologies, and, as their name says, are created from solids.

To take advantage of the large polarization achievable at liquid–solid interfaces, solid-state field-effect transistors (FETs) are already being fabricated in which the gate dielectric consists of water gels[2] or solid-state electrolytes such as water-infiltrated nanoporous $12CaO \times 7Al_2O_3$ glass.[3] Moreover, liquid-gated graphene FETs have been fabricated by coating the graphene to position millimeter-sized droplets of NaCl aqueous solutions as gate dielectrics on sample surfaces.[4] Numerous devices have furthermore been successfully manufactured in which gels were printed or photo-patterned (see, e.g., refs. [5,6]). In these devices and in the pioneering electrolyte-gated FETs,[7–18] liquids and solids were combined to enhance functional properties or to achieve new ones. Further progress resulting from combining liquids and solids in devices could be accelerated if it were possible to integrate liquids into solid-state heterostructures. The liquids would be protected from interacting with the atmospheric environment, and by using thin-film technologies small volumes of different liquids could be positioned at microscopically defined locations. The idea of genuine integration of liquids in solid heterostructures such as illustrated in Figure 1, has—to our knowledge—not yet been pursued. The basic question is how liquids can be patterned and overgrown with solid layers. Here we demonstrate successful integration of liquids into heterostructure devices and report on their properties and potential.

The path we have explored to solve both problems of patterning the liquids and overgrowing them is to first grow solid precursors of the liquids, and then to liquefy them after heterostructure growth. Solid–liquid transitions may, for example, be achieved for specific compounds by cracking chemical bonds with photon irradiation. In the work discussed here, we implemented a cryogenic process and deposited

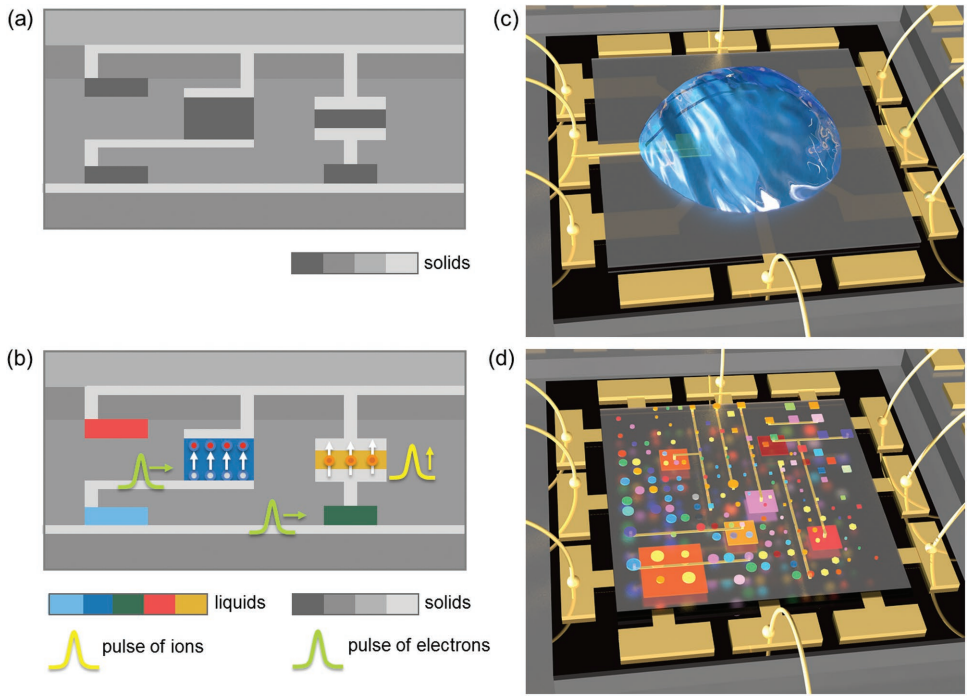


**Figure 1.** Schematics of integrated heterostructures comprising functional liquids. a) Exemplary cross section of a solid-state heterostructure comprising several materials. b) Sketch of envisioned solid-state/liquid-state heterostructures. Analogous to (a), this cross section illustrates the freedom of design and advances achievable if microscopic volumes of liquids (colored) were integrated into heterostructures. In the liquid volumes, for example, ions may create electric double layers (center) or move across gaps (sketch at right). c) Illustration of a typical state-of-the-art sample setup used for ionic gating. A macroscopic drop of an electrolyte (blue) dropped onto the sample provides the gate liquid. d) Sketch illustrating the vision of a sample containing integrated, microscopic liquid volumes, as opposed to (c). Different liquids patterned into distinct shapes may be placed onto the sample at well-determined locations and then overgrown by subsequent layers.

frozen liquid which we subsequently melted and restructured (Figure S1, Supporting Information; Experimental Section). To explore the feasibility and potential of heterostructures with integrated liquids, we implemented integrated electric double-layer capacitors and integrated liquid-gated FETs as test vehicles. We selected the liquid for its compatibility with film growth processes, and to offer large polarizations and fast switching. These requirements are fulfilled by water (see, e.g., ref. [13]) and NaCl aqueous solutions, which can be grown by thermal evaporation, have polarizations of several μF $cm^{-2}$ and switching delays below 100 μs (Figure S2a, Supporting Information). Control experiments were performed by using macroscopic drops applied to large parts of the device surface (Supporting Information). This is the process used today to fabricate liquid-gated FETs, for example, to explore phase transitions in quantum matter (see, e.g., refs. [10,15–17,19–24]).

Integration of liquids into heterostructure using our cryogenic process required optimization of device architectures, materials, and growth conditions (see Experimental Section) to overcome the following three key challenges: i) encapsulating the liquid such as to withstand the liquid–solid volume change and the thermal expansion differences, ii) forming contacts at the liquid–solid interface over the microsized areas available, and iii) avoiding undesirable motion of the liquid during sample fabrication. Nanoscale characterization of the surfaces and interiors of test devices by cryo-scanning electron microscopy (cryo-SEM) and cryo-focused ion beam (cryo-FIB) techniques, which preserve the frozen liquids, showed the aqueous solution to be intact and present in the desired areas throughout the interior of the investigated devices (**Figure 2**a).

A typical capacitor chip contains devices of various sizes. If operated below the threshold voltage of water decomposition (1.23 V), the devices performed over hundreds of measurement cycles reproducibly for 2 weeks, including several cycles of freezing and warming. As known from bulk samples, the device characteristics showed slight drifts in consecutive measurement sweeps, consistent with the time needed for $Na^+$ and $Cl^-$ ions to relax in the bulk aqueous solution, the original behavior being recovered again when remeasuring the devices after a day or sloshing the device gently. After 2 years of unattended storage in air on a shelf, the capacitors showed nominally the characteristics of the devices after 2 weeks of experimenting (**Figure 3**). The room-temperature capacitances (5–40 μF $cm^{-2}$) far exceeded those achieved with the bulk-drop technique (≈2–3 μF $cm^{-2}$), but varied over a wider range. From their measured electric properties, we conclude that this variation is mainly caused by the electrolyte in some devices not being in contact with the full area of an electrode. Additional variations likely originate from differences of the NaCl concentrations in the device liquids. The high values of the capacitances agree with those of an electric double layer. In a control measurement, we cooled the devices below the freezing temperature. The capacitance collapsed by a factor of 20–25 to the value expected for the parasitic capacitance of the circuits, thus demonstrating that water had been successfully

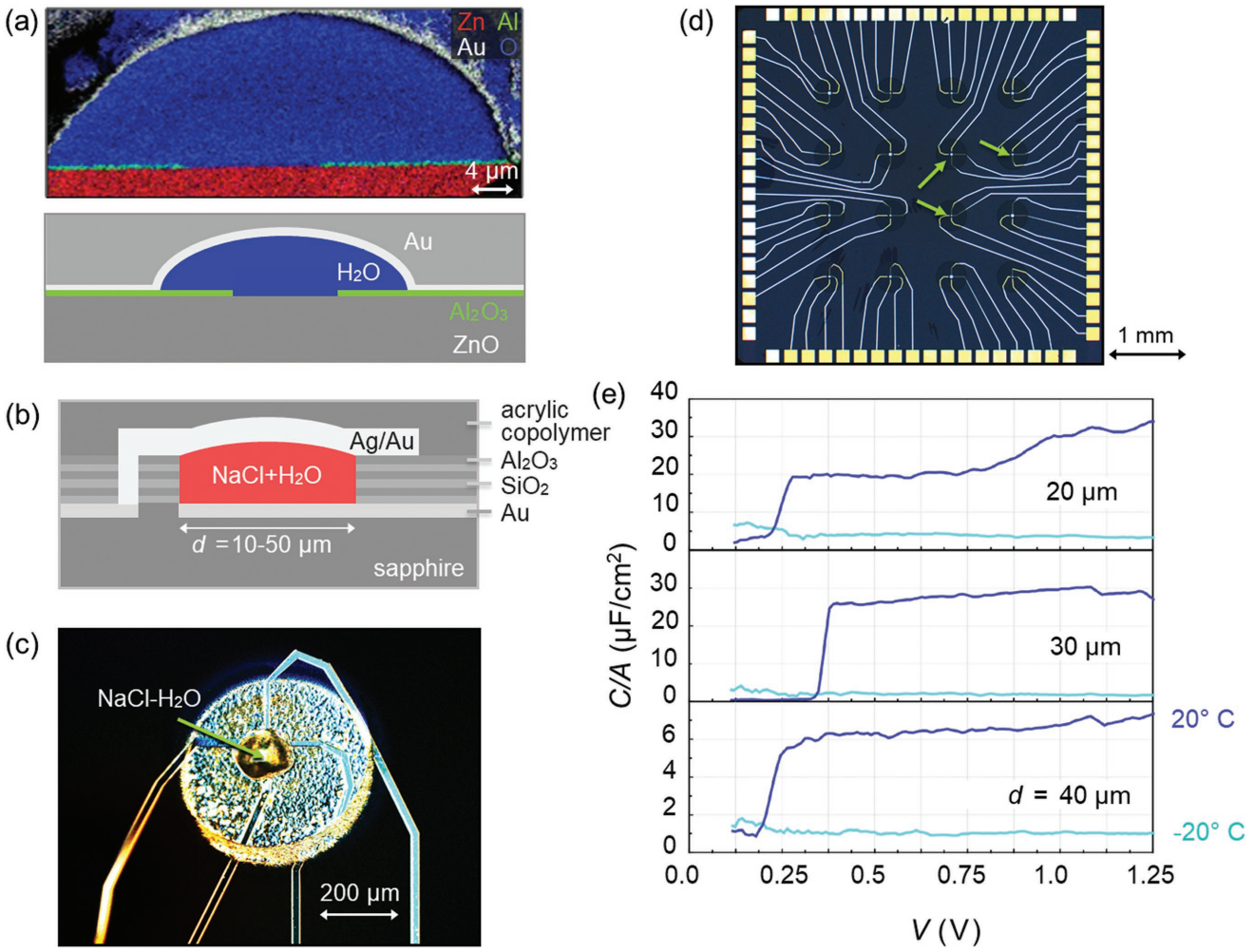


**Figure 2.** Capacitors with integrated liquids. a) Cryo energy-dispersive X-ray (Cryo-EDX) map of a cross-sectional cut of a test sample after cryo-FIB milling, revealing an $Al_2O_3$ isolation layer at the solid–liquid interface. The dark contrast at the top-right Au–liquid interface is due to the EDX detector location which gives rise to shadowing. The lower panel shows a sketch of the cross section. b) Sketch of a cross section (not to scale) of capacitors with integrated NaCl–$H_2O$ fabricated. c) Optical microscopy image of a capacitor with an integrated NaCl–$H_2O$ dielectric of ≈20 μm diameter (green arrow). d) Photograph of a sample with 16 integrated capacitors after deposition of NaCl, before $H_2O$ deposition. The green arrows point to three of the capacitors (small bright dots). e) Areal capacitances of three capacitors with integrated NaCl–$H_2O$ and diameters of 20, 30, and 40 μm measured as a function of applied voltage. Freezing the water causes the capacitances to collapse to the stray value.

integrated into electrolytic capacitor devices. Surprisingly, unlike the bulk-droplet devices, the $C(V)$ characteristics of the integrated capacitors in various samples consistently displayed a step-like behavior (Figure 2e). At voltages of 0.2–0.4 V, the capacitance increases in a step from the parasitic capacitance to the double-layer capacitance (Figure 2e; Figure S3, Supporting Information). Such steps are followed by a continuous increase of the capacitance with increasing voltage. We attribute the steps to the presence of small vapor pockets in the devices, likely caused by the volume reduction of $H_2O$ during the melting step. The liquid–solid interface is formed only outside the pocket. The increasing voltage pulls the liquid to the solid as known from electrowetting,[25] thereby increasing the effective area of the liquid–solid interface, see, for example, Figure S4 (Supporting Information). Steps are also seen in the characteristics of several integrated FETs (**Figure 4**c), in the same voltage range as for the capacitors.

Using this process, we fabricated FETs with liquids integrated into the gate stacks (see Figure 4a). The samples were grown on ZnO, which served as channel material. ZnO FETs with bulk liquid-drop gates have already been explored[10] and found to have excellent characteristics. The chips contained 10–20 FETs (Figure 4b). This number was determined by boundary conditions of our setup, and should not suggest any limit to the possible integration level. The liquids had volumes of ≈10 × 10 × 10 μm$^3$ ($w \times l \times h$), and the channel lengths of the FETs equaled 10 μm. Figure 4c shows the room-temperature output characteristic $I_D(V_{DS})$ of such an integrated FET. The characteristics are in good agreement with those of conventional ZnO FETs gated by bulk drops of $H_2O$–NaCl. On–off ratios exceed 100 (≈20 for the bulk devices), and gate currents are negligible (<20 nA; Figure S5, Supporting Information). The devices tended to show a sizable hysteresis of the $I_D(V_{DS})$ characteristics, as is common for electrolyte-gated FETs.

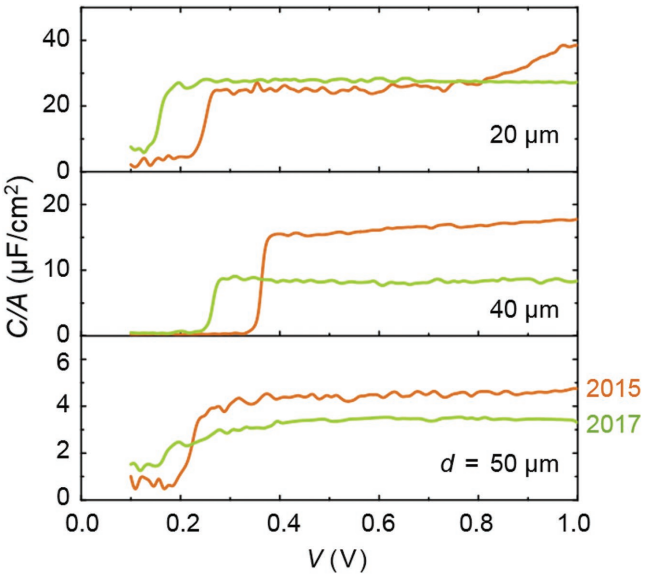


**Figure 3.** Areal capacitances of three capacitors with integrated NaCl–$H_2O$ and diameters of 20–50 μm measured at room temperature as a function of applied voltage before and after storing them for 2 years at room temperature, in air.

Interestingly, analogous to the switching behavior displayed by the $C(V)$ characteristics of the capacitors, the FETs display a hysteretic switching of the drain currents, reminiscent of memristors.[26] This behavior of the drain currents is consistent with a similar behavior reported for water-gated $MoS_2$ FETs[27,28] and is to be expected as the $H_2O$ molecules in direct contact with the drain-source channel act as charge scattering and trapping centers.

Compared to the standard layout of electrolyte-gated FETs that use open and large drops of electrolytes covering large sample areas, integrating the electrolytes by thin-film technologies opens the possibility to enhance the reproducibility of the fabrication process and keep the electrolytes clean and protected from the atmosphere. Geometrical factors and the environment of the liquid may be controlled with high precision so that several different electrolytes may be used in immediate spatial proximity. Reducing the liquid volumes may offer a route to increase the switching frequency of the devices.

We have investigated the potential and possibilities of merging integrated circuit technology with liquids by exploring, as examples, chips containing integrated capacitors and FETs. Patterned liquids integrated into solid-state heterostructures offer novel possibilities for science and applications. Challenges of incorporating liquids into solid-state heterostructures are given by enhanced complexity of the device fabrication, and—as we have found—new set of challenges on device stability, arising, for example, from the interdiffusion of ions, thermal expansion, and formation of vapor pockets. Any new technology needs to proceed through several phases while transitioning from explorations in research laboratories to real-life applications. We hope that with the next generation of devices enabling novel research applications, experience will be gained for first simple devices to be used in commercial applications, for example, in ionotronics.

For the future, we foresee the implementation of a large variety of liquids patterned to even finer scales, possibly even into the nanoscopic regime, integrated into heterostructures of

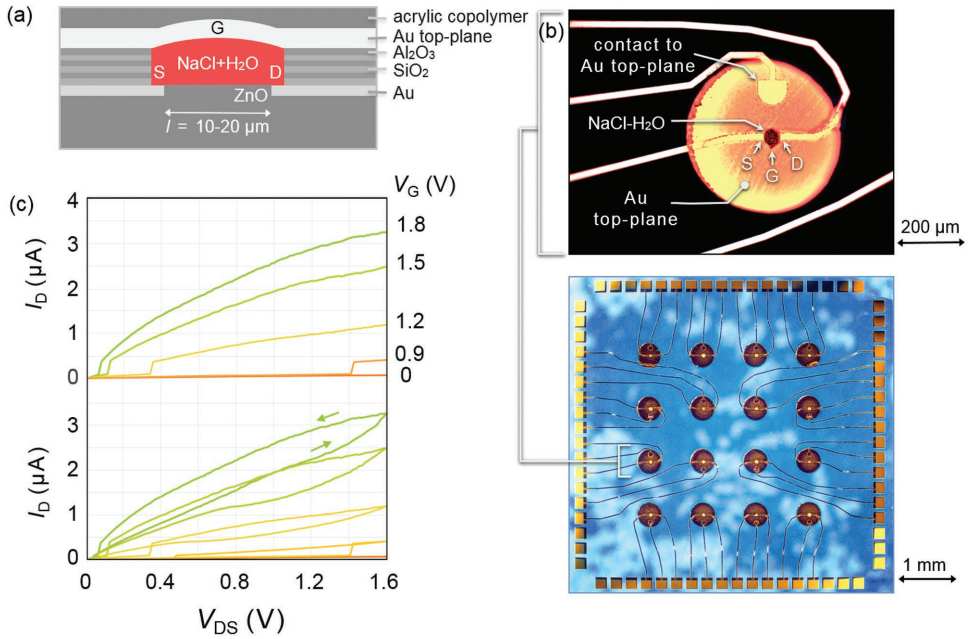


**Figure 4.** Field-effect transistors with integrated liquids. a) Sketch showing a cross section (not to scale) of field-effect transistors with integrated NaCl–$H_2O$ fabricated. b) Top: Optical microscopy images of a ZnO-field-effect transistors with integrated NaCl–$H_2O$ dielectrics (arrow). These transistors have channel lengths $l \approx 10$–20 μm. Bottom: optical microscopy images of a chip containing 16 FETs in accordance with (a). The FET of line 3, row 1 is shown in the top panel. c) Typical switching characteristics of such FETs measured at room temperature. For clarity, the upper figure shows the characteristics for falling drain-source voltages only. During all measurements, the gate currents were smaller than 25 nA.

high complexity. By qualitatively extending the available spectrum of mechanical, electronic, and functional properties available, the incorporation of liquids into integrated circuits opens a hitherto unavailable phase space for circuit architecture. The capability of integrating liquids on the nanoscale into solid-state heterostructures will ultimately lead to mesoscopic fluids and mesoscopic liquid particles, which we expect to be of fundamental interest by enabling new applications of nanoionics.[29] By utilizing ion transport and the design possibilities for liquids in heterostructures, this novel device concept links integrated circuits, adaptive electronics, biology, solid-state chemistry, and neuromorphic computing. Integrated liquids pave the way to nanoscale chemical modifications of heterostructures, which utilize the liquids as sources and sinks of ions,[17,29,30] thus creating new possibilities for simultaneous electronic and ionic transport for processing energy and information.

## Experimental Section

*Sample Design and Growth Methods*: An essential step toward realizing FETs was to test the process of fabricating integrated capacitors as shown in Figure 2b–d and Figure S6 (Supporting Information). For the side walls confining the liquid, we found it important to grow $SiO_2$ (20 nm)-$Al_2O_3$ (30 nm) × 3 superlattices instead of simple oxide monolayers because the superlattices provide enhanced mechanical strength in contact with the electrolyte. The top layer of an acrylic copolymer was deposited after growth to enhance the stability of the devices during thermal cycling and to provide additional protection of the devices' surfaces.

Fabrication steps of the integrated liquid capacitors and FETs

1. Preparation of ZnO substrates by annealing in oxygen for 4 h at 500 °C. Fabrication of bottom contacts by thermal deposition of Ti (15 nm)/Pt (15 nm)/Au (15 nm) on ZnO (for transistors) or on $Al_2O_3$ (for capacitors) substrates. Patterning of bottom contacts by optical lithography of photoresist and lift-off.
2. Growth of [$SiO_2$ (20 nm)/$Al_2O_3$ (30 nm)] × 3 multilayers by thermal evaporation. Patterning by optical lithography of photoresist and lift-off.
3. Deposition of ≈ 35 nm NaCl by thermal evaporation. Patterning by lifting-off photoresist with acetone.
4. Deposition of $H_2O$ by thermal evaporation through shadow mask, substrate temperature –60°C, thickness ≈2–5 µm. Formation of the NaCl aqueous solution on the areas covered by NaCl by annealing for ≈2 min at room temperature and 1 bar of $N_2$.
5. Ar-ion milling (≈$1 \times 10^{-4}$ mbar, 5 min, –170°C) to clean water-free areas.
6. Fabrication of ≈100 nm top contacts by thermal evaporation of Ag, Au, or Ag/Au through shadow mask. Sample temperature: –170 °C, growth rate ≈5 Å $s^{-1}$.
7. Deposition of protection layer consisting of acrylic copolymer (2-butoxyethanol (5–10%), 2-methoxy-1-methylethylacetate (1–5%), acetone (30–60%), butane (5–10%), isobutane (1–5%), propane (10–30%)), and adhesion promoter on desired areas at room temperature.

*Capacitance Measurements*: All data shown in the main text of the manuscript have been gained from dc-measurements of the capacitance between the bottom contact (Au) and the top metallic layer (Ag/Au) that encapsulates the liquid (as described, see also Figure 2b). A Keithley 237 Source-Measure unit was used for the dc-measurements. The ac-measurements shown in Figure S2 (Supporting Information) were performed by using an LCR-meter (Agilent E4980A, 20 Hz–2 MHz) with excitation voltages in the order of 100 mV.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

B.P., G.P., and J.M. designed, and B.P. and G.P. built the setups for sample preparation and measurements. B.P., G.P., and E.F.-T. fabricated and characterized the devices; M.J.Z. and L.F.K performed the cryo-FIB/SEM and cryo-EDX measurement of the sample, and all authors analyzed data. J.M. developed the idea and guided the research. All the authors gratefully acknowledge discussions with H. D. Abruña, H. Boschker, D. Fischer, T. Harada, M. Jäger, R. Kjellander, H. Klauk, J. Maier, H. J. Mannhart, J. Popovic, and C. Schön. M.J.Z. and L.F.K. acknowledge support by the NSF (DMR-1654596) and the David and Lucile Packard Foundation. This work made use of the Cornell Center for Materials Research Shared Facilities which are supported through the NSFMRSEC program (DMR-1719875).

## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

electrolyte gating, field-effect transistors, heterostructures, patterning liquids

Received: April 23, 2018
Revised: June 11, 2018
Published online: July 17, 2018

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